

## iMS4-L -xxx (revB) Modular Quad Output Synthesizer

## **Overview and Functions**

Models -

| Model      | Outputs | Feature                             | Frequency     | RF Output |
|------------|---------|-------------------------------------|---------------|-----------|
|            |         |                                     | Range (MHz)   | Power     |
| iMS4-L     | 4       | Standard model                      | 12.5 – 200MHz | 1.2mW     |
| iMS4-L-Fx2 | 4       | Integrated Frequency doubling stage | 150 - 400MHz  | 50mW      |
|            |         |                                     |               |           |
|            |         |                                     |               |           |
|            |         |                                     |               |           |

iMS4-L-Fx2 is a discontinued product

Options -xxx, combinations possible

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## Supporting Documents:

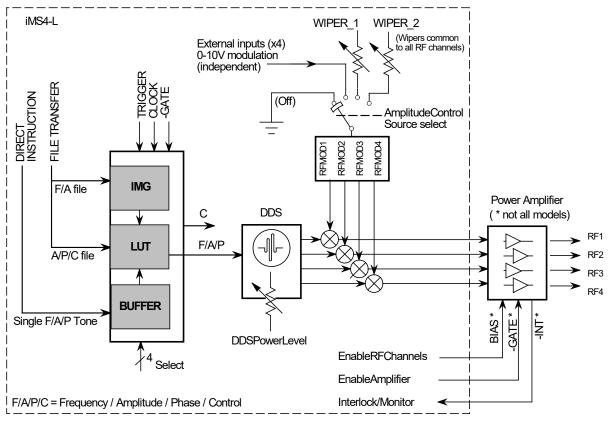
Isomet iMS4 GUI Software Guide

Compensation LUT Explanation and Generation Guide



## 1. Hardware Overview and Key features.

The diagram below illustrates a schematic of the iMS4-L connected with a generic Power Amplifier **Before** operating the IMS4-L, it will be necessary to load the USB Window drivers. (See section 10). The IMS4-L operates from DC power and requires a 15V-24Vdc supply (0.7A at 24Vdc)



Conceptual diagram for iMS4-L with PA



The iMS4 synthesizer operates in three basic modes

## **1.1** Local Tone Buffer (LTB) or Single Tone Mode.

This mode is useful for setting the AO Bragg Angle or switching rapidly between 256 preassigned points. The DDS synthesizer generates a single tone output at the specified Frequency, Amplitude and Phase or F/A/P triad.

Key features:

- Up to 95 KHz update rate.
- The required output tone may be selected via software control or from hardwired inputs.
- Option to bypass the LUT modifier (see LUT description below)

## **1.2 IMAGE mode or Sequence mode.**

This mode is useful for generating larger more complex scan patterns.

An Image file (IMG) containing the desired frequency scan pattern is downloaded into memory space within the iMS4-L. Output play back is under the control of user defined Image Trigger and Image Clock.

Key features:

- Update rate up to 330KHz, all four channels.
- Any frequency pattern may be generated e.g. random, linear, step, saw tooth.
- Image may contain up to 4096 frequency points across 4 outputs.
  - i.e. 1024 points if all four outputs are programmed. (For larger capacity, see iMS4-P)

LUT and Image files can be generated on Excel Spread sheets and imported into the C++ project.

## 1.3 Enhanced tone mode (Ramp / Step mode)

This mode uses the inherent sweep functions built into the DDS chip. Frequency, amplitude\*\* or phase can be ramped in value.

## **Control Features**

## Look-up-table (LUT)

A calibration or compensation look-up-table (LUT) contains frequency specific phase and amplitude data. Its purpose is to compensate for non-linearity and non-uniformities in the wider system. E.g. create efficient uniform intensity scan lines in an AOD base laser scanning system.

Initial values for the LUT are calculated and loaded into the IMS prior to running the Local Tone Buffer or Image modes. Subsequently, LUT values may be modified with real world measured data or integrated within a feedback mechanism.



## Amplitude and Power Level control

Each frequency point is assigned a unique 10-bit amplitude value ranging from 0 -100% of the maximum RF power setting. This is a <u>relative value</u> and is dynamic i.e. able to change from output point to output point.

The maximum RF output power setting is defined by the iMS AmplitudeControl and DDSPowerLevel digital potentiometers. These are 8-bit static controls and together define the <u>absolute</u> RF power level of the IMS4-L (and any connected power amplifier module).

## Auxiliary Digital and Analog I-O signals

The iMS-L also features:

| Signal Description  | <u>Ident</u>                          |
|---|---------------------------------------|
| 12 bit Synchronous output register, updated with the each new image point,  | SDOR[011]                             |
| 10 bit Asynchronous output,   | GP Out[110]                           |
| 8 bit Asynchronous input,   | GP In[18]                             |
| 1 bit 24V PLC compatible opto relay output,   | Laser bit                             |
| 2x Synchronous analog outputs, 0 -5V full scale<br>1x Asynchronous analog output, 0 -10V full scale<br>2x Asynchronous analog inputs, 0 -10V full scale | AOUT_FrqAmp<br>AOUT_DAC<br>Aux_ADC1 2 |

## Main operating modes and functions.

Please refer to the application program interface (API) documentation with the software development kit (SDK) available as a download.

## 2. Single (Set Calibration) Tone.

Simplest mode. Direct programming of the DDS frequency, amplitude and phase values. Bypasses LUT compensation.

## 3. Local Tone Buffer.

The Local tone buffer (LTB) area contains a maximum 256 F/A/P locations. The 256 F/A/P Tones may be rapidly addressed using 8x external LTB address lines or directly from the operating software.

| LTB ext'l address, J8<br>(pins 3,4,5,6,16,14,7,8). | Function            | Update rate |
|--|---------------------|-------------|
| 0 h FF h   | Select Tone address | 10.5usec    |

The compensation look up table (see below) may be applied to the Tone Buffer output if required.



## 4. Enhanced Tone Mode (Ramp / Step mode)

This mode uses the inherent sweep functions built into the DDS chip.

Frequency, amplitude\*\* or phase can be ramped in value. For conciseness, only frequency ramps and steps will be described.

## 4.1 Ramp Mode

A ramp or chirp is generated by rapidly incrementing the frequency. The number of increment steps and duration of the ramp are user programmable. Each output can be programmed with different ramp parameters.

The ramps are initiated from the GUI or applying a signal to the external Profile inputs on connector J8

Available functions:

- Independent Up Down ramp slopes.
- Dwell (stop at end value) or no-dwell (return to start value) at end of sweep duration.
- Set amplitude value for ramp. (remains constant for the ramp duration).

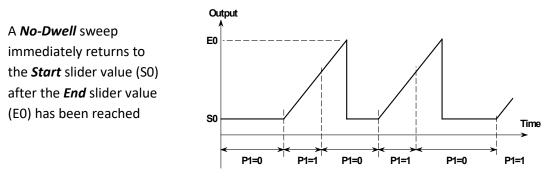
The Ramp mode offers the fastest frequency sweep capability, with a minimum dwell time of 8nsec per frequency increment.

Independent sliders for each of the four output channels define:

- Duration of the rising slope increment.
- Duration of the falling slope increment.
- The number of points for each ramp, up or down.

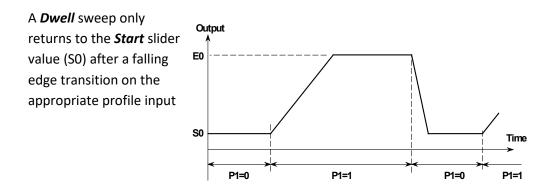
The falling slope only applies if 'Dwell' is selected in the *Mode* pull down menu.

A **Frequency Sweep no dwell** immediately returns to the start value after the end value has been reached



A **Frequency Sweep Dwell** only returns to the start value after a falling edge transition on the appropriate profile input



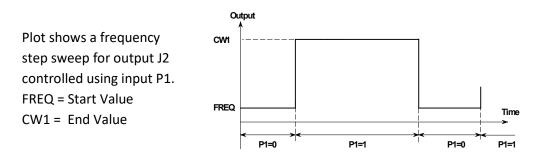


Both plots show a ramp on output J2, controlled using input P1

(\*\*An internal limitation in the DDS chip prevents amplitude ramps in the Enhanced tone mode).

## 4.2 Step mode

This is essentially a two-level sweep or two-level modulation. Step mode may be applied to the Frequency, Amplitude or Phase. Dwell/No dwell has no function.



## Amplitude

The amplitude level across a Frequency or Phase sweep (or step) remains a constant. The value is set by a combination of the **DAC Current** level buttons (Full , ½, ¼, ¼) and the sliders on the **Signal Path** panel.



## 5. Image Mode.

An Image contains multiple F/A/P data points pre-arranged to give the desired frequency or scan pattern. Image playback is initiated with the Image Trigger. The output update rate is determined by the Image Clock. The Image trigger and clock may be software generated or applied from an external source. At each clock edge, the next location in the Image Memory area is addressed. The frequency and amplitude data point is read and modified by the LUT data (see below). The resultant F/A/P triad is routed to the DDS registers. An update clock is then issued to the DDS and all 4x RF outputs are simultaneously updated with a new Frequency, Amplitude and Phase value. Any Synchronous control data will also be updated on the appropriate I/O port.

Multiple images can be grouped together into a play sequence. Each image within a sequence can have unique properties such as clock rate and post image delay. Likewise multiple sequences can be defined and queued. These are uploaded into the iMS DDR memory and played in FIFO order. Memory is dynamically allocated to permit flexibility in the size and number of both the images and sequences, and to allow simultaneous upload and output of data. The total number of images (excluding repeats) is 4096. The size of a single image is in excess of a 1million F/A/P points.

## 6. Look-up-table (LUT).

The LUT is frequency-addressed look-up-table for applying amplitude and phase compensation to the RF signal output. The tables are indexed by the nearest programmed LUT frequency to the demanded output frequency. Table entries are linearly spaced in frequency from the lowest to highest supported. The number of entries in the table is hardware specific. At a minimum, the LUT must contain amplitude compensation data over the desired frequency range of interest.

LUT Size: 2047 entries equally spaced from 12.5 – 200MHz.

Primary features: Compensation Data

•Amplitude: a value between 0 and 100% for modifying the output amplitude according to frequency. Used for compensating for AOD efficiency as well as filter attenuation and DDS roll-off.

•Phase: 0 - 360 degrees. Represents the per-channel phase difference applied to enable beam steered (= phased array) applications. Value represents the phase offset between adjacent channels Channel 1 is the reference and unmodified. Channel 4 will exhibit the largest phase differential relative to Channel 1.

Secondary features: Synchronous output data

•Sync Analog: A value between 0.0 and 1.0 that can be output on one of the synchronous DAC outputs (updated in step with the RF image point data).

•Sync Digital: A binary value that can be output on the synchronous digital outputs (updated in step with the RF image point data).



## 7. RF power Level and Modulation.

The output RF power at each frequency is determined by the combination of static controls and point specific amplitude data values.

**Static Asynchronous Controls.** Applies to all operating modes. Purpose: To set the maximum safe operating RF power level.

 DDS Power Level. 8-bit non-volatile digital pot. Always programmed.
 Sets the DDS chip output level using a dedicated digital pot. Common to all outputs. Typical values 50 – 90%

#### << and >>

- 2: Amplitude Control Source for the RF mixers, 4 options. Must select and apply one.
- 00: OFF. Common to all outputs
- 01: EXTERNAL signal(s)\*, per RF channel, output proportional to applied control voltage.
- 10: WIPER\_1, internal 8-bit non-volatile digital pot setting. Common to all outputs
- 11: WIPER\_2, alternative to Wiper\_1

The value written and stored to Wiper\_1 (or Wiper\_2) sets the RF mixer drive level. Typical values 50 – 100%

The above controls should be set in combination so that the AO device is operated at optimum efficiency without saturating the connected power amplifiers and/or applying excessive RF power to the AO device. Starting values will be provided on the appropriate test data sheets

(\* Can be wired together to combine multiple channels onto a common control input. 0-10V, 600-ohm / channel. May also used for fast asynchronous amplitude modulation).

## Dynamic Synchronous Control.

Purpose: To set or modulate the RF power at a specific output frequency. (i.e. to control the diffracted laser intensity at a specific scan angle)

3: <u>Tone Buffer mode</u>

The 10-bit amplitude data value associated with a specific frequency value. This is multiplied by the LUT amplitude calibration factor for that frequency point.

<< or >>

## 4: <u>Image mode</u>

The 10-bit amplitude data value associated with a specific frequency value. This is multiplied by the LUT amplitude compensation factor for that frequency point.



For a typical AO scanning application, the Image amplitude data is a simple "On" or "Off" value. The LUT is programmed with the variable amplitude compensation data that creates the desired weighting for the scan intensity profile.

In both cases, the LUT can be bypassed if required. The LUT is applied by default.

## 8. Technical Specifications.

#### Image Mode

| Timing                           | Value    | Condition   |
|----------------------------------|----------|---|
| Frequency Settling Time          | < 40nsec | Step change in Image data value                     |
|                                  |          | (Phase accumulator set to clear at each DDS update) |
| Output Delay to Image Clock edge | 1.6 usec | * 0.25usec  |
| Minimum Trigger to Clock edge    | TBD nsec |   |
| Maximum Image Clock rate         | 300 KHz  | * 1MHz (See iMS4-P)                                 |
| Minimum Image Clock rate         | 0 Hz     |   |

| GATE, TRIGGER, CLOCK inputs. J9, J10, J11 | Value        | Condition       |
|---|--------------|-----------------|
| Absolute Maximum Input Voltage            | 5.5V         | Per input.      |
| Recommended Input Voltage                 | 3V < Vh < 5V | Vh = logic High |
| Minimum Input Voltage                     | 0V           |                 |

Active edge of the external Clock or Trigger inputs is user programmable . Default = rising

\* Future planned optimization. Please contact Isomet

## Local Tone Buffer Mode

| Timing                            | Value    | Condition   |
|-----------------------------------|----------|---|
| Frequency Settling Time           | < 40nsec | For tone – tone selection                           |
|                                   |          | (Phase accumulator set to clear at each DDS update) |
| Output Delay - LTB address change | 6 usec   |   |
| Maximum LTB address rate          | 95KHz    |   |
| Minimum LTB address rate          | 0 Hz     |   |

| LTB address, input Voltages, J8           | Value        | Condition       |
|---|--------------|-----------------|
| Absolute Maximum Input Voltage            | 5.5V         | Per input.      |
| Recommended Input Voltage,                | 3V < Vh < 5V | Vh = logic High |
| Minimum Input Voltage                     | 0V           |                 |
| Opto-isolated, signal source sink current | 16mA         | Per input       |



## **External Modulation Inputs, J8**

| Parameter                       | Value    | Condition                                |
|---------------------------------|----------|--|
| RF output rise time             | < 40nsec | Step change in external modulation input |
| Output Delay - Modulation input | 50nsec   | Step change in external modulation input |
| Absolute Maximum Input Voltage  | 12V      | Per input.                               |
| Recommended Input Voltage       | 10V      |  |
| Minimum Input Voltage           | 0V       |  |
| Input impedance                 | ~600Ω    | Per input                                |
| On:Off ratio                    | > 35dB   | Full range                               |
| Maximum modulation rate         | 10MHz    |  |
| Minimum modulation rate         | 0 Hz     |  |

## **RF power control, SDK**

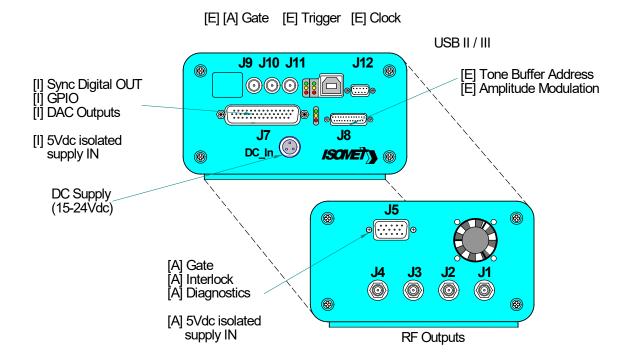
| Max – Min                                       | Full Range | Condition                        |
|---|------------|----------------------------------|
| DDS Power Level                                 | 8dB        | All other variables at max power |
| Amplitude Control Source : Wiper_1, _2 or Ext'l | 39dB       |                                  |
| Image or LTB Amplitude data                     | 48dB       | 10bit range                      |
|   |            |                                  |

## RF outputs, J1,J2,J3,J4

| RF Output                    | Full Range      | Condition     |
|------------------------------|-----------------|---------------|
| Maximum output power         | > 1.2mW / 0.8dB | At 80MHz,     |
| Frequency Stability          | 25ppm           | -40C to +85C  |
| Spurious output              | > 40dBc         |               |
| Harmonics                    | > 25dBc         | At 1mW output |
| Channel to Channel Isolation | > 43dB          | At 1mW output |



#### 9. Hardware Connection.



Minimum Connections:

- USB II or USB III to a host PC.
- DC Supply, 15V / 1A minimum to 24V / 0.5A maximum
- One or more RF outputs, as required.

#### Recommended channel connections

| AOD / Amplifier Channels | iMS Outputs                           |
|--------------------------|---------------------------------------|
| Single                   | Any                                   |
| Dual                     | J1, J2 or J3, J4                      |
| Quad                     | All, in ascending or descending order |

Optional connections are identified as follows:

[E] = hardwired control signals from external signal source(s).

Functionally equivalent software generated control signal are provided in the SDK.

[I] = opto-isolated IO buffered signals requiring an external 5Vdc supply connection to J7 or J8

[A] = external power amplifier connections (see explanation below)

The iMS4-L features external power amplifier diagnostic and control signals. These are available on J5. J5 will require 5V opto isolator dc feed (5V\_RFA) from the connected RF amplifer. An appropriate interface card must exist within the power amplifier.



#### Basic amplifier control

With few exceptions, most Isomet existing power amplifier modules require an active low Gate or Enable signal to operate and will output a normally closed over-temperature thermal interlock signal.

#### **Diagnostics**

Certain amplifier models include diagnostic outputs indicating:

- Forward and reflected RF power (between the PA outputs and connected AO device/load).
- Temperature of the PA
- DC current
- Temperature of the AO device

These are communicated via I2C bus on J5.

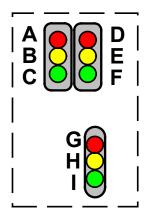
Examples include:

| Model         | Channels | Power/ch  | Frequency Range | Enable/Gate<br>Control | Diagnostics |
|---------------|----------|-----------|-----------------|------------------------|-------------|
| 500C series   | 1        | 2,4,or 7W | Model dependent | NA                     | NA          |
| 800PC-f/f/f/f | 4        | 1W        | Model dependent | NA                     | NA          |
| RFA200-2H     | 2        | 100W      | 35 – 65         | J5                     | NA          |
| RFA1170-4     | 4        | 80W       | 48-92           | J5                     | J5          |
| RFA0110-2-20  | 2        | 20W       | 90-130          | J5                     | J5          |
| RFA0120-4-15  | 4        | 15W       | 100-120         | J5                     | J5          |
|               |          |           |                 |                        |             |

NA= not applicable



## 10. LED Indicators.



## Top Stack, Controller PCB

| Ident | LED             | Mode           | iMS4-L                        |
|-------|-----------------|----------------|-------------------------------|
| A     | RED (top left)  | If illuminated | Not Downloading File          |
| В     | Yellow          | If illuminated | Downloading File              |
| С     | Green           | Pulsing        | Controller OK                 |
| D     | RED (top right) | If illuminated | Image output stopped          |
| E     | Yellow          | If illuminated | Waiting on Trigger            |
| F     | Green           | If illuminated | Image playing / output active |

## Lower stack. Synthesizer PCB

| Ident | LED       | Mode        | Stand Alone    | In combination with PA and          |
|-------|-----------|-------------|----------------|-------------------------------------|
|       |           |             | iMS4-          | J5 is connected                     |
| G     | RED (top) | Constant on | DC power On    | Thermal Interlock Open (= fault)    |
| Н     | Yellow    | Constant on | NA             | PA is enabled. Thermal Interlock OK |
| I     | Green     | Pulsing     | Synthesizer OK | Synthesizer OK                      |

#### DC power applied, USB communication problem

If the 6x LED's (A,B,C,D,E,F) are constantly illuminated, then USB communication has not been established. In this case:

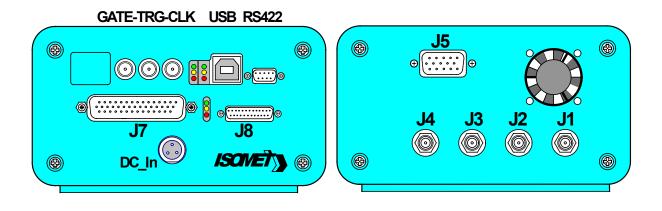
- a: Ensure USB driver is loaded (see section 10)
- b: Cycle DC power

and /or

c: Disconnect then reconnect USB

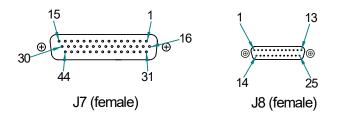


## 11. Connector pin-outs.



## D-type pin idents looking into connector

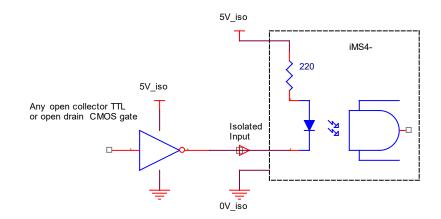
Front panel view



Pin-out descriptions as follows:

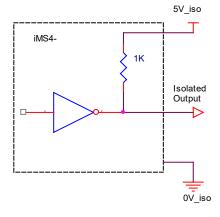
Circuit details for opto-isolated inputs / outputs on J7 and J8 connector

Recommended drive circuit for opto-isolated logic inputs

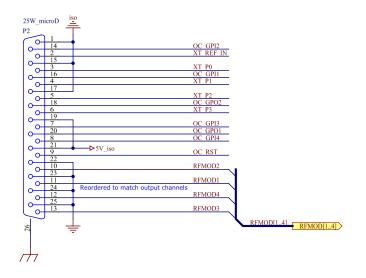




Opto-isolated logic output schematic



## J8, 25way micro-D connector



# Main connection for external control signals (Micro-D to full size D-type converter cable available).

| Connector     | Туре   | 25way micro-D       |                                    |               |            |
|---------------|--------|---------------------|------------------------------------|---------------|------------|
|               | Ident  | J8                  |                                    |               |            |
| <u>Signal</u> | Signal | <u>Type</u>         | Description                        | Alternate use | <u>Pin</u> |
| Designation   |        |                     |                                    |               |            |
| RFmod4        | In     | Analog, 0-10V       | External amplitude control for RF4 |               | 12         |
| A_Rtn         |        | Analog              | Analog return                      |               | 24         |
| RFmod3        | In     | Analog, 0-10V       | External amplitude control for RF3 |               | 13         |
| A_Rtn         |        | Analog              | Analog return                      |               | 25         |
| RFmod2        | In     | Analog, 0-10V       | External amplitude control for RF2 |               | 10         |
| A_Rtn         |        | Analog              | Analog return                      |               | 22         |
| RFmod1        | In     | Analog, 0-10V       | External amplitude control for RF1 |               | 11         |
| A_Rtn         |        | Analog              | Analog return                      |               | 23         |
| RST           | In     | Opto isolated logic | Reset                              |               | 9          |
| REF_IN        | In     | Opto isolated logic | Reference Frequency (Optional)     |               | 2          |

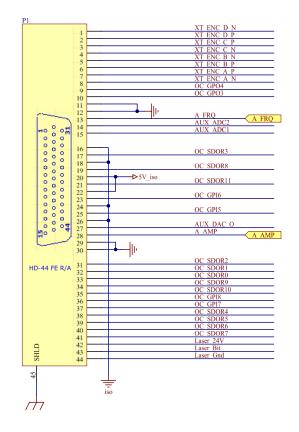
#### AN180823: iMS4-L rev-B Overview and Functions



|                |     | or or open drain gate, 16m<br>nternal 1Kohm pull-up to 5 |                                   | LTB = Local Tone Buffer    |    |
|----------------|-----|--|-----------------------------------|----------------------------|----|
| Type Logic = T |     |  |                                   | GP = General Purpose       |    |
| Notes:         |     |  |                                   | Кеу:                       |    |
| D_Rtn          | DC  |  | isolated OV / signal return input | 0V                         | 17 |
| 5V_iso         | DC  |  | Isolated 5V DC supply input       | 5V output, 10mA            | 21 |
| 5V_iso         | DC  |  | Isolated 5V DC supply input       | 5V output, 10mA            | 19 |
|                |     |  |                                   |                            |    |
| D_Rtn          | DC  |  | isolated 0V / signal return input | 0V                         | 15 |
| D_Rtn          | DC  |  | isolated 0V / signal return input | 0V                         | 1  |
| P3             | In  | Opto isolated logic                                      | Profile select, bit3              | LTB location/address, bit3 | 6  |
| P2             | In  | Opto isolated logic                                      | Profile select, bit2              | LTB location/address, bit2 | 5  |
| P1             | In  | Opto isolated logic                                      | Profile select, bit1              | LTB location/address, bit1 | 4  |
| PO             | In  | Opto isolated logic                                      | Profile select, bit0              | LTB location/address, bit0 | 3  |
| D_Rtn          | DC  |  | isolated 0V / signal return input | 0V                         | 17 |
| GP O2          | Out | Opto isolated logic                                      | Async general purpose output      |                            | 18 |
| GP 01          | Out | Opto isolated logic                                      | Async general purpose output      |                            | 20 |
| GP I4          | In  | Opto isolated logic                                      | Async general purpose input       | LTB location/address, bit7 | 8  |
| GP 13          | IN  | Opto isolated logic                                      | Async general purpose input       | LTB location/address, bit6 | 7  |
| GP 12          | In  | Opto isolated logic                                      | Async general purpose input       | LTB location/address, bit5 | 14 |
| GP I1          | In  | Opto isolated logic                                      | Async general purpose input       | LTB location/address, bit4 | 16 |

## J7, 44way high density-D connector

Connection for auxiliary I-O signals



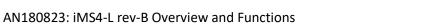


| Connector         | Туре       | 44way HD-D               |   |                      |         |
|-------------------|------------|--------------------------|---|----------------------|---------|
|                   | Ident      | J7                       |   |                      |         |
| Signal            | Signal     | Type                     | Description                                 | Alternate use        | Piı     |
| Designation       |            |                          |   |                      |         |
| SDOR0             | Out        | Opto isolated logic      | Synchronous-Digital Output bit0             |                      | 33      |
| SDOR1             | Out        | Opto isolated logic      | Sync-Digital Output bit1                    |                      | 32      |
| SDOR2             | Out        | Opto isolated logic      | Sync-Digital Output bit2                    |                      | 31      |
| SDOR3             | Out        | Opto isolated logic      | Sync-Digital Output bit3                    |                      | 17      |
| SDOR4             | Out        | Opto isolated logic      | Sync-Digital Output bit4                    |                      | 38      |
| SDOR5             | Out        | Opto isolated logic      | Sync-Digital Output bit5                    |                      | 39      |
| SDOR6             | Out        | Opto isolated logic      | Sync-Digital Output bit6                    |                      | 40      |
| SDOR7             | Out        | Opto isolated logic      | Sync-Digital Output bit7                    |                      | 41      |
| SDOR8             | Out        | Opto isolated logic      | Sync-Digital Output bit8                    |                      | 19      |
| SDOR9             | Out        | Opto isolated logic      |   |                      | 34      |
|                   | +          |                          | Sync-Digital Output bit9                    |                      | +       |
| SDOR10            | Out        | Opto isolated logic      | Sync-Digital Output bit10                   |                      | 35      |
| SDOR11            | Out        | Opto isolated logic      | Sync-Digital Output bit11                   |                      | 21      |
| D_Rtn             | Out        |                          | isolated 0V / signal return input           | 0V                   | 26      |
| DL4_N             |            | 5V differntial logic     |   |                      | 1       |
| DL4_N             | In         | 5V differntial logic     | <u> </u>                                    |                      | 2       |
| DL3 P             | In         | 5V differntial logic     | +   |                      | 3       |
| DL3_F             | ln         | 5V differntial logic     | +   |                      | 4       |
| DL3_N             | ln         | 5V differntial logic     | +   |                      | 5       |
| DL2_N<br>DL2 P    | ln         | 5V differntial logic     |   |                      | 6       |
| DL1 P             | In         | 5V differntial logic     |   |                      | 7       |
| <del>-</del>      | +          | 5V differntial logic     |   |                      |         |
| DL1_N<br>D_Rtn    | ln<br>In   | (5V iso supply required) | isolated 0V / signal return input           | 0V                   | 8<br>16 |
|                   |            | (01_100 00pp1) (0quileu) |   |                      |         |
| GP 15             | In         | Opto isolated logic      | Asynchronous GP logic input                 |                      | 25      |
| GP 16             | In         | Opto isolated logic      | Async GP input                              |                      | 23      |
| GP 17             | In         | Opto isolated logic      | Async GP input                              |                      | 37      |
| GP 18             | In         | Opto isolated logic      | Async GP input                              |                      | 36      |
| GP 03             | Out        | Opto isolated logic      | Async GP logic output                       |                      |         |
| GP 04             | Out        | Opto isolated logic      | Async GP output                             |                      | 10      |
| D_Rtn             | Out        | Opto isolated logic      | isolated 0V / signal return input           |                      | 24      |
| <u>-</u>          |            |                          |   |                      |         |
| 24V_laser         | In         | PLC                      | Laser Opto-Supply                           |                      | 42      |
| Laser_Bit         | Out        | PLC                      | Laser Opto relay bit Tr/Tf < 50usec)        |                      | 43      |
| Gnd_laser         | In         | PLC                      | Laser Opto-Gnd                              |                      | 44      |
|                   |            | Analaa                   |   |                      | 10      |
| AOUT_Frq          | Out        | Analog                   | 8-bit analog representation of Image freq   |                      | 13      |
| AOUT_Amp          | Out        | Analog                   | 8-bit analog equivalent of Image amplitude  |                      | 28      |
| A_Rtn             | Out        | Analog                   | Analog return                               |                      | 30      |
| AOUT_DAC          | Out        | Analog                   | GP 12-bit DAC analog output.                |                      | 27      |
| A_Rtn             | Out        | Analog                   | Analog return                               |                      | 29      |
| Aux_ADC1          |            | Analog                   | GP Analog input to a 12-bit ADC (0 to 10V). |                      | 15      |
| A Rtn             | In         | Analog                   | Analog return                               |                      | 11      |
| Aux_ADC2          | In         | Analog                   | GP Analog input to a 12-bit ADC (0 to 10V). |                      | 14      |
| Aux_ADC2<br>A_Rtn | In         | Analog                   | Analog return                               |                      | 12      |
|                   |            |                          |   |                      |         |
| 5V_iso            | DC         |                          | Isolated 5V DC supply input                 | 5V output, 10mA      | 22      |
| 5V_iso            | DC         |                          | Isolated 5V DC supply input                 | 5V output, 10mA      | 20      |
| D_Rtn             | DC         |                          | isolated 0V / signal return input           | 0V                   | 18      |
| Notes:            |            |                          |   | Kov                  |         |
|                   | or 5V CMOS | <u> </u>                 |   | GP = General Purpose |         |
| Type Logic = TTL  |            |                          |   |                      | 1       |



## **Other Connectors**

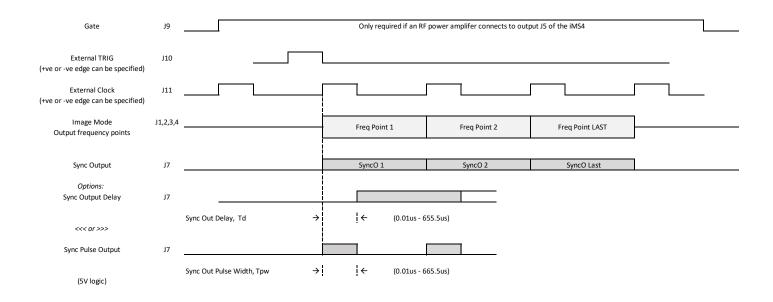
| Connector   | Туре     | see table           |                                   |               |             |          | ļ      |
|-------------|----------|---------------------|-----------------------------------|---------------|-------------|----------|--------|
|             | Ident    | see table           |                                   |               |             |          |        |
| Signal      | Signal   | Type                | Description                       | Alternate use | Connector   | Ident    | Pin    |
| Designation | <u></u>  | <u>.,,,,,</u>       |                                   |               |             |          |        |
|             |          |                     | Communication                     |               |             |          | 1      |
| NOT USED    | na       | na                  | na                                |               | RJ45        |          | 1      |
| USB Serial  | In/Out   | Logic               | USB II / USBIII                   |               | B-type      | -        | +      |
|             |          |                     |                                   |               |             |          |        |
| RX-P        | In       | Logic               | RS422 receive+                    |               | 9-way D     | J12      | 2      |
| RX-N        | In       | Logic               | RS422 receive-                    |               | 9-way D     | J12      | 1      |
| TX-P        | Out      | Logic               | RS422 transmit+                   |               | 9-way D     | J12      | 7      |
| TX-N        | Out      | Logic               | RS422 transmit-                   |               | 9-way D     | J12      | 6      |
| Rtn         | Gnd      |                     | Sig Rtn                           |               | 9-way D     | J12      | 5      |
|             |          |                     |                                   |               |             |          |        |
|             |          |                     | DC Supply                         |               | 2           |          |        |
| Vdc         | DC<br>0V | DC-In               | Supply 15V -24V dc, <0.4A         |               | 3w TINI-Q   |          | 1      |
|             | UV       | DC-In               |                                   |               | 3w TINI-Q   |          | 2      |
|             |          |                     | SMA Coax Connections              |               |             | +        | +      |
| Gate        | In       | Logic               | Enable power amplifiers via J5    | POF input     | SMA coaxial | J9       | Centre |
| Rtn         | Gnd      | 208.0               | Sig Rtn                           | i or input    |             |          | Outer  |
|             |          |                     |                                   |               |             |          |        |
| Trigger     | In       | Logic               | Trigger Image Data Output         | POF input     | SMA coaxial | J10      | Centre |
| Rtn         | Gnd      |                     | Sig Rtn                           |               |             |          | Outer  |
|             |          |                     |                                   |               |             |          |        |
| Clock       | In       | Logic               | Clock Image Data                  | POF input     | SMA coaxial | J11      | Centre |
| Rtn         | Gnd      |                     | Sig Rtn                           |               |             |          | Outer  |
|             |          |                     |                                   |               |             |          |        |
| Ch0         | Analog   | RF                  | RF1 frequency output, 50 $\Omega$ |               | SMA coaxial | J1       | Centre |
| Rtn         | Gnd      |                     | Sig Rtn                           |               |             |          | Outer  |
| Ch1         | Analog   | RF                  | RF2 frequency output, 50 $\Omega$ |               | SMA coaxial | J2       | Centre |
| Rtn         | Gnd      |                     | Sig Rtn                           |               |             |          | Outer  |
| Ch2         | Analog   | RF                  | RF3 frequency output, 50 $\Omega$ |               | SMA coaxial | J3       | Centre |
| Rtn         | Gnd      |                     | Sig Rtn                           |               |             |          | Outer  |
| Ch3         | Analog   | RF                  | RF4 frequency output, 50 $\Omega$ |               | SMA coaxial | J4       | Centre |
| Rtn         | Gnd      |                     | Sig Rtn                           |               |             |          | Outer  |
|             |          |                     |                                   |               |             |          |        |
|             |          |                     | J5 Power Amp Control *            |               |             |          |        |
| 5V_RFA      | In       |                     | Opto supply from connected PA     | 5V, 20mA out  | 15w-HD D    | J5       | 1      |
| 5V_RFA      | In       |                     | Opto supply from connected PA     | 5V, 20mA out  | 15w-HD D    | J5       | 10     |
| OV_RFA      | In       |                     | Opto 0V from connected PA         | 0V            | 15w-HD D    | J5       | 4      |
| 0V_RFA      | In       |                     | Opto 0V from connected PA         | 0V            | 15w-HD D    | J5       | 7      |
| SCL_RFA_TX  | 10       | Opto isolated logic | I2C Clock_TX                      |               | 15w-HD D    | J5       | 2      |
| SCL_RFA_RX  | 0        | Opto isolated logic | I2C Clock_RX                      |               | 15w-HD D    | J5<br>J5 | 3      |
| SDA_RFA_TY  | 10       | Opto isolated logic | I2C Data TY                       |               | 15w-HD D    | J5<br>J5 | 5      |
| SDA_RFA_RY  |          | Opto isolated logic | I2C Data RY                       |               | 15w-HD D    | J6       | 6      |
|             |          |                     |                                   |               |             |          |        |
| EXT-CONVST  | Out      | Opto isolated logic | Start ADC conversion              |               | 15w-HD D    | J5       | 8      |
| -EXT_GATE   | Out      | Opto isolated logic | Enable connected amplifier        |               | 15w-HD D    | J5       | 9      |
| EXT-BSY     | In       | Opto isolated logic | ADC conversion busy               |               | 15w-HD D    | J5       | 11     |
| EXT-INT_MON | In       | Opto isolated logic | Interlocks valid monitor          |               | 15w-HD D    | J5       | 12     |
| ·····       |          |                     |                                   |               |             |          | 1      |





## 12. Signal Timing Diagram

## Applies to Image mode





## 13. Software.

The core of the Software Development Kit is the C++ iMS library and API. All interaction with iMS hardware ultimately passes through this API. However we have also provided a number of other software utilities and wrappers that allow you to use the iMS System at a higher level of abstraction.

Included in the SDK are:

- •The core iMSLibrary binaries for a number of different platforms and toolsets.
- •Accompanying C++ header files for application interface.

•iMSNET An experimental .NET assembly written in C# that wraps the core library and permits user application development in any .NET language targeting the .NET Framework

•ims\_hw\_server is a command line daemon type process that can handle all communication with an iMS system, decoupling it from user application business logic. A gRPC streaming interface connects the server to application software, either on the same host or across a network.

•iMS Studio is a full featured GUI front end application that can be used to create Images, Tone Buffers and Compensation Functions and play them on an iMS system. This is often a good starting point for users wishing to explore the capabilities of an iMS before starting development of custom software.

The iMS software is available for download from https://isomet.com/ims4\_sw.html Depending on your computer select and run one of the following :

Isomet iMS SDK v 1.xx Win7 Setup.exe Isomet iMS SDK v 1.xx Win10 Setup.exe

The software download also includes documentation and tutorials for setting up a project and connecting to the iMS. Note: these Tutorials are NOT specific to any practical AO device.

Please refer to Quick Start Guide: Isomet iMS Studio for instructions on the Isomet Windows GUI

The iMS software library and API has been written purely in native ANSI-C++ with some use of features introduced in C++11 (ISO/IEC 14882:2011), including the C++ Standard Library. There is no use of features associated with the updated C++14 specification.

Isomet will provide example projects applicable to the customer hardware configuration.

The Software Development Kits are regularly updated. Please check for Isomet website for updates.



## a. Visual Studio Notes

|  | Visual Studio 20 | 13 (v120) | Visual Studio 2015 (v140) |        |
|--|------------------|-----------|---------------------------|--------|
| 32-bit   |                  | 64-bit    | 32-bit                    | 64-bit |
| Microsoft Windows<br>2000/XP/Vista or<br>earlier | ×                | ×         | ×                         | ×      |
| Microsoft Windows<br>7 Professional              | 1                | 1         | 1                         | 1      |
| Microsoft Windows<br>8/8.1                       | Δ                |           |                           | Δ      |
| Microsoft Windows<br>10 Professional             | ×                | ×         | 1                         | 1      |

#### b. Folder locations.

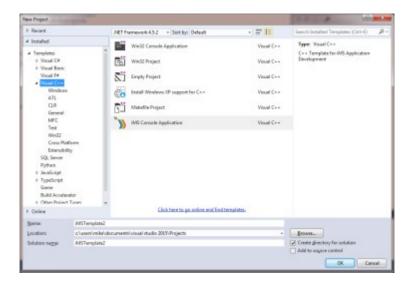
For ease of installation, a C++ console application template file is provided.

Copy the file *iMSTemplateWin7VC140.zip* into the Visual Studio project templates folder e.g. C.....Documents > Visual Studio 2015 > Templates > ProjectTemplates

DO NOT unzip

| leganics * Shara with * Du | am New folder                          |                  | • 1 0        |
|----------------------------|--|------------------|--------------|
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| Downloads                  | Name                                   | Date readfied    | Type         |
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| Homegroup                  |  |                  |              |
| a normagnap                |  |                  |              |
| Computer                   |  |                  |              |
| Local Disk (C)             |  |                  |              |

When starting *New Project* from Visual Studio, the *iMS Console Application* will be offered Edit the <u>Name</u> and project <u>Location</u> as required



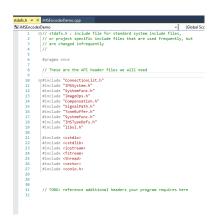


#### c. Adding C++ code to the project template

Please refer to the comments within the C++ template code and the ReadMe.txt file

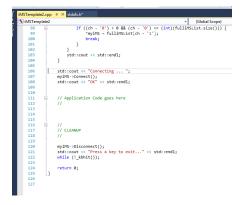
The application includes the example code necessary for connection to the iMS4 (via selected ports) and files which are used to build a precompiled header (PCH) file; StdAfx.h, StdAfx.cpp

Add additional include files to StdAfx.h only



Referencing the default Source file (e.g. iMSTemplate.cpp)

User application code is added from line 111





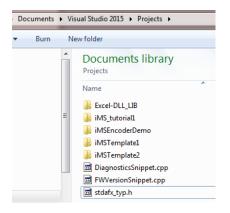
## d. Installing the 3<sup>rd</sup> party Excel Spreadsheet Import Export function

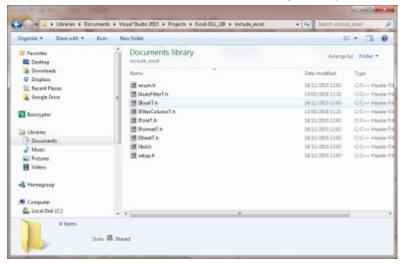
Generating Compensation Tables (LUTs) and Image files in Excel can be convenient. Several routines exist to import data into C++. One such is from libxl.com A licence key is required and it is free to use. Add the following code prior to calling the LibXL functions.

// call LibXL licence key
libxl::Book\* ExcelBook = xlCreateBook();
ExcelBook->setKey(L"Michael Hillier", L"windows-222329040ec5ec046fb46767a7h1gej6");

To add this feature to your project

Create a folder Excel-DLL\_LIB in the Projects folder and download associated files (contact Isomet)





• Add the above additional include files to *StdAfx.h* only

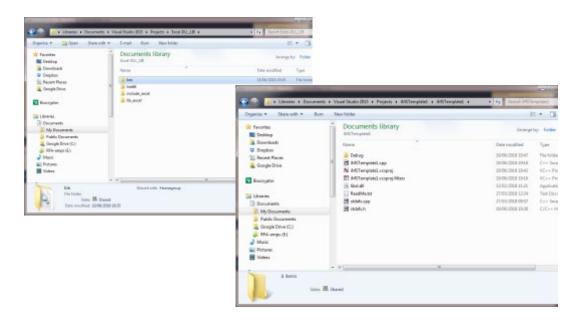


Add 'include\_excel' to the above Additional Include Directory under C++ > General.

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• Copy libxl.dll from > Excel\_DLL-LIB > bin to the project folder you created.

It must be in the same folder as the source file \*.cpp.





• Add the folder containing libxl.lib to the *Additional Library Dependencies* under *Linker > General*.

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• Add libxl.lib to the *Additional Dependencies* under *Linker > Input* 

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## 14. Direct programming of the DDS Synthesizer Chip.

For most applications, the use of the DDSscript function is not required.

## Use with CAUTION

The DDS IC that generates the RF signals can be manually programmed to access advanced features that wouldn't normally be available through the iMS API. To do this requires a detailed knowledge and understanding of the Analog Devices AD9959 Frequency Synthesiser IC and its register map.

If it is necessary to manually program the AD9959, a sequence of register writes can be generated (called a DDS Script) and stored in the Synthesiser Filesystem. The application software may then recall the script from the filesystem and execute it to commit the register writes to the AD9959. Please refer to DDSscript Class description in the SDK documentation.

## **REGISTER MAPS**

Each register write is initialised with the name of the register as the first argument. (This is in the same abbreviated form as specified in the AD9959 datasheet).

| Register<br>Name                                 | Bit<br>Range | Bit 7<br>(MSB)                                    | Bit 6                                      | Bit 5   | Bit 4                                      | Bit 3                          | Bit<br>2   | Bit1   | Bit 0<br>(LSB) | Default<br>Value         |
|--|--------------|---|--|---|--|--------------------------------|------------|--|----------------|--------------------------|
| (Serial<br>Addr)                                 | Nunge        | (1135)  |  |   |  |                                | -          |  | (150)          | Value                    |
| Channel<br>Select<br>Register<br>(CSR)<br>(0x00) | [7:0]        | Channel 3<br>Enable *<br>(1 = On)                 | Channel 2<br>Enable *                      | Channel 1<br>Enable *                             | Channel 0<br>Enable *                      | Must<br>be 0                   | Se         | al I/O mode<br>lect [2:1]<br>2 <b>=1, B1=0</b> | LSB first      | 0xF4<br>DO NOT<br>CHANGE |
| Function<br>Register 1<br>(FR1)<br>(0x01)        | [23:16]      | VCO gain<br>control                               |  | PLL divide  |  | Charge pump<br>Control [17:16] |            |  |                |                          |
|  | [15:8]       | Open  | Profile pi                                 | in configuration (PP                              | Ramp-up<br>(RU/RD) [                       |                                | Modulation | Modulation level [9:8]                         |                |                          |
|  | [7:0]        | Reference clock<br>input power-<br>down           | External power-<br>down mode               | SYNC_CLK<br>disable                               | DAC reference<br>power-down                | Open [3:2]                     |            | Manual<br>hardware<br>sync                     | Manual<br>sync | 0x00                     |
| Function<br>Register 2                           | [15:8]       | All channels<br>autoclear<br>sweep<br>accumulator | All channels<br>clear sweep<br>accumulator | All channels<br>autoclear<br>phase<br>accumulator | All channels<br>clear phase<br>accumulator | Open [1                        | 1:10]      | Open [9:8]                                     |                | 0x20                     |
| <b>(FR2)</b><br>(0x02)                           | [7:0]        | Auto sweep<br>sync<br>enable                      | Multidevice sync<br>master enable          | Multidevice<br>sync<br>status                     | Multidevice sync<br>mask                   | Open [3:2]                     |            | System clock offset<br>[1:0]                   |                | 0x00                     |

#### **Control Register Map**

Defaults = Power -on hard coded DDSScript

\* Channel enable bits do not require an I/O update to be activated.

These bits are active immediately after the byte containing the bits is written.

All other bits need an I/O update to become active.

These four channel enable bits are used to enable/disable any combination of the four channels. The default is all four enabled.



#### Channel Register Map

| Register<br>Name<br>(Serial<br>Addr)                        | Bit<br>Range | Bit 7<br>(MSB)                          | Bit 6                     | Bit 5                            | Bit 4                             | Bit 3                      | Bit 2                             | Bit1                                 | Bit 0<br>(LSB)                   | Default<br>Value |  |  |
|---|--------------|---|---------------------------|----------------------------------|-----------------------------------|----------------------------|-----------------------------------|--------------------------------------|----------------------------------|------------------|--|--|
| * Channel<br>Function<br>Register<br><b>(CFR)</b><br>(0x03) | [23:16       | Amplitude fre<br>(AFP) select           |                           | Open [21:16]                     |                                   |                            |                                   |                                      |                                  |                  |  |  |
|   | [15:8]       | Linear sweep<br>no-dwell                | Linear<br>sweep<br>enable | Load SRR at<br>I/O_UPDATE        | Open                              | [12:11]                    | Must be 0 DAC full-scale current  |                                      |                                  | 0x03             |  |  |
| ()  | [7:0]        | Digital<br>power-<br>down               | DAC<br>power-<br>down     | Matched<br>pipe delays<br>active | Autoclear<br>sweep<br>accumulator | Clear sweep<br>accumulator | Autoclear<br>phase<br>accumulator | Clear<br>phase<br>Accumul<br>ator ** | Sine<br>wave<br>output<br>enable | 0x00             |  |  |
| * Channel<br>Frequency                                      | [31:24]      | Frequency Tuning Word 0 [31:24]         |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| Tuning<br>Word 0  | [23:16]      | Frequency Tuning Word 0 [23:16]         |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| (CFTW0)   | [15:8]       | Frequency Tuning Word 0 [15:8]          |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| (0x04)  | [7:0]        | Frequency Tuning Word 0 [7:0]           |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| * Channel<br>Phase  | [15:8]       | Open [15:14] Phase Offset Word 0 [13:8] |                           |                                  |                                   |                            |                                   |                                      | 0x00                             |                  |  |  |
| Offset<br>Word 0<br>( <b>CPOW0</b> )<br>(0x05)              | [7:0]        | Phase Offset Word 0 [7:0]               |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| Amplitude<br>Control  | [23:16]      | Amplitude ramp rate [23:16]             |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| Register<br>(ACR)<br>(0x06)                                 | [15:8]       | Increment/decr<br>size [15:             |                           | Open                             | Amplitude<br>multiplier<br>enable | Ramp-up/<br>down<br>enable | Load ARR at<br>I/O_UPDATE         | Amplitu<br>Factor                    |                                  | 0x13             |  |  |
|   | [7:0]        | Amplitude scale factor [7:0]            |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| * Linear<br>Sweep   | [15:8]       | Falling sweep ramp rate (FSRR) [15:8]   |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| Ramp<br>Rate<br>(LSRR)<br>(0x07)                            | [7:0]        | Rising sweep ramp rate (RSRR) [7:0]     |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| * LSR Rising<br>Delta                                       | [31:24]      | Rising delta word [31:24]               |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| Word  | [23:16]      | Rising delta word [23:16]               |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| ( <b>RDW)</b><br>(0x08)                                     | [15:8]       | Rising delta word [15:8]                |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
|   | [7:0]        | Rising delta word [7:0]                 |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| * LSR<br>Falling  | [31:24]      | Falling delta word [31:24]              |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| Delta<br>Word   | [23:16]      | Falling delta word [23:16]              |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| (FDW)   | [15:8]       | Falling delta word [15:8]               |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |
| (0x09)  | [7:0]        | Falling delta word [7:0]                |                           |                                  |                                   |                            |                                   |                                      |                                  |                  |  |  |

\*\* The clear phase accumulator bit is set to Logic 1 after a master reset. It self-clears or is set to Logic 0 when an I/O update is asserted.

\* There are four sets of channel registers and profile registers, one per channel. The addresses of all channel registers and profile registers are the same for each channel. The channel enable bits (Control Register 0, CSR [7:4]) determine if the channel registers and/or profile registers of each channel are written to or not.



## **Profile Register Map**

For clarity, only the MSB byte is shown for each Channel Word register.

| Register<br>Name                       | Bit<br>Range | Bit 7<br>(MSB) | Bit 6           | Bit 5           | Bit 4       | Bit 3        | Bit 2     | Bit1         | Bit 0<br>(LSB) | Default<br>Value |
|--|--------------|----------------|-----------------|-----------------|-------------|--------------|-----------|--------------|----------------|------------------|
| Channel Word 1 (CW1) (0x0A)            | [31:0]       |                | requency tuning | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 2 (CW2) (0x0B)            | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 3 (CW3) (0x0C)            | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 4 ( <b>CW4</b> ) (0x0D)   | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 5 ( <b>CW5</b> ) (0x0E)   | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 6 (CW6) (0x0F)            | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 7 ( <b>CW7</b> ) (0x10)   | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 8 ( <b>CW8</b> ) (0x11)   | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 9 ( <b>CW9</b> ) (0x12)   | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 10 ( <b>CW10</b> ) (0x13) | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 11 ( <b>CW11</b> ) (0x14) | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 12 ( <b>CW12</b> ) (0x15) | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 13 (CW13) (0x16)          | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 14 ( <b>CW14</b> ) (0x17) | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |
| Channel Word 15 (CW15) (0x18)          | [31:0]       | I              | requency tunin  | g word [31:0] c | r Phase wor | d [31:18] or | Amplitude | word [31:22] |                | N/A              |

Each channel word register has a capacity of 32 bits (only 8 shown above).

If phase or amplitude is stored in the channel word registers, it must be first MSB aligned per the bit range.

## File System

Once created, DDSScripts can be downloaded to the filesystem on the Synthesiser (they can only be committed to the AD9959 from the file system, they cannot be executed directly. Create a DDSScriptDownload object initialised from the DDSScript and the attached iMS, then call the .Program() function to transfer the contents. The function parameters assign a file name (max 8 chars) to the script stored in the Filesystem, and indicate whether it should be executed at power-up (DEFAULT) or not (NON\_DEFAULT). This second argument is optional, if not given, it will be set to NON\_DEFAULT. Note that only one script in the Filesystem can be set to DEFAULT.